Wafer-Level Thinned Monolithic CMOS Imagers in a Bulk-CMOS Technology

Bedabrata Pain, Chao Sun, Paula Vo, Bruce Hancock, Thomas J. Cunningham,
Chris Wrigley, Risaku Toda, Victor White, Amrita Banerjee*, and Durgmadhab Misra*
Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
Phone: 818-354-8765; Fax: 818-393-0045; Email: bpain@jpl.nasa.gov
* Dept of Electrical & Computer Engineering, New Jersey Institute of Technology
161 Warren St, Newark, NJ 07102

As the pixel pitch of CMOS image sensors continue to shrink, there is a growing recognition of the advantages of back-illuminated image sensors [1,2], such as improved sensitivity, angular response, integration of process electronics in the pixel, and easier process integration with newer back-end-of-the-line. This paper builds on our previous work [1], and describes the design, fabrication, and test results on a monolithic 1024x1024 back-illuminated digital CMOS imager as well as on diode test structures, both fabricated on SOI silicon wafers with a built-in oxide etch-stop layer for wafer-level thinning.

In a back-illuminated image sensor, light is coupled from the side opposite to where the devices are fabricated, and after the wafer substrate has been thinned to an appropriate thickness. Despite its use in scientific image sensors, there remain a number of challenges for monolithic back-illuminated image sensor fabrication [3,4]: These include (a) accurate and uniform wafer-level thinning, (b) surface passivation following thinning, (c) wafer support during thinning, and, (d) pad opening and packaging.

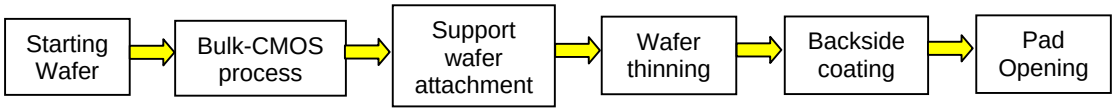

Figure 1: Schematic back-thinned imager process flow

The basic monolithic back-illuminated imager fabrication process is schematically shown in figure 1. It consists of the fabrication of a CMOS imager using an imager-compatible bulk-CMOS process on a SOI wafer. The finished wafer is attached to a second wafer for support during thinning, followed by wafer-level thinning using an oxide etch-stop. This is followed by the application of appropriate coatings on the backside of the wafer. The final step in the process is opening the pads and dicing the wafers into individual chips. The individual chip-pads are wire-bonded for electrical I/O.

Figure 2 shows the schematic cross-section of the imager wafer prior to thinning, with the substrate of the wafer facing up (the direction of optical collection). It consists of a SOI wafer as a starting material with a high-resistivity (~60 Ω-cm) p-type device layer that is 10 µm thick, and is separated from the handle wafer substrate by a 0.3 µm thermally grown high quality buried oxide (BOX) layer. The CMOS imager, designed with an 8 µm pixel-pitch, was fabricated with a 0.25 µm 4metal bulk-

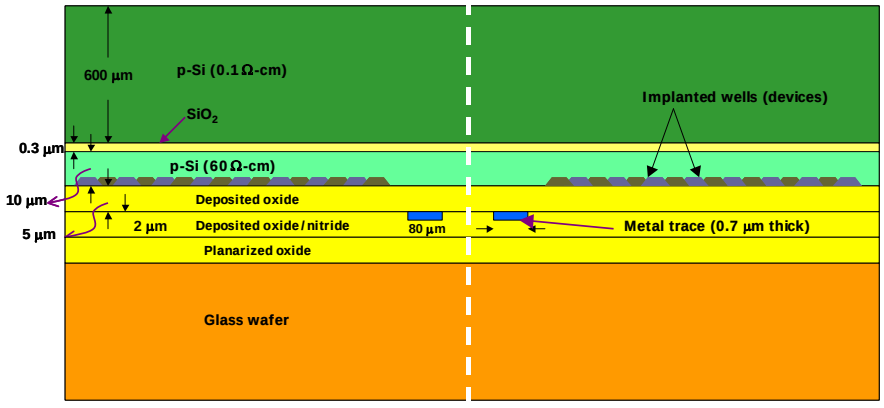

Figure 1: Schematic cross-section of the imager after glass wafer is bonded to the finished wafer (imager wafer shown upside down)

CMOS technology. The test structures were fabricated at New Jersey Inst. of Tech. 1 μm CMOS process.

The back-end-of-the-line (BEOL) consists of a 7 μm thick metal and inter-level dielectric stack, with a planarized deposited oxide being the final step. The bond-pads (indicated at metal trace in figure 1) - 80 μm wide and 0.7 μm thick - are embedded in the ILD stack. The white dashed line indicates the dicing channel separating two adjacent dies. The handle-wafer provides mechanical support during device fabrication, but is eventually etched away as part of the back-side thinning process that uses the buried oxide as an etch-stop to complete wafer-level thinning.

The finished device wafer is mounted on a glass wafer that provides mechanical support during thinning. We have used two different approaches for bonding the glass wafer – one, using a UV-cured glue and secondly, by using a room-temperature oxide-to-oxide wafer-bonding method [5]. The latter method is preferable, since it allows post-thinning anneal at 400 ^{o}C – not readily possible when adhesives are used.

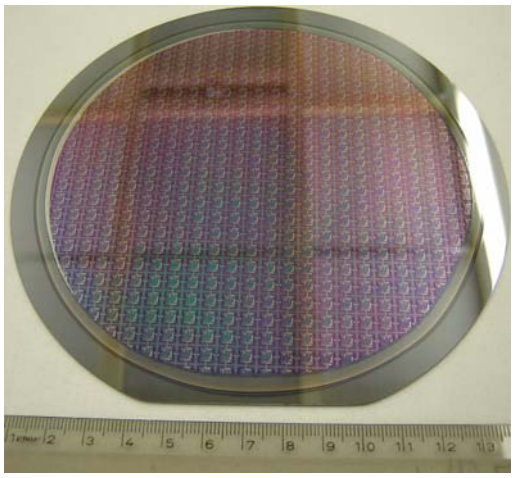

Figure 2: Picture of the room-temperature bonded wafers (device wafer can be seen through the glass wafer)

By using the room-temperature oxide-to-oxide bonding method, we successfully bonded 150 mm diameter finished device wafers consisting of planarized oxide-on-top to glass wafers with low sodium content. The glass wafer has an extremely small surface-roughness (~ 20A), and the deposited oxide is planarized using CMP < 20A measured surface roughness. Prior to room-temperature bonding, the oxides at the bonding surfaces were chemically activated [6], followed by a long duration annealing at 175^{o}C for bond-strengthening and the elimination of voids. High-temperature annealing is ruled out, since this is being carried out post-BEOL. The bond strength even with lower temperature anneal was found to be strong enough to withstand dicing of the wafer into pieces ranging from 3mm^2 to 100 mm^2 without any delamination. Figure 2 shows picture of the bonded wafers, indicating void-free bonding across the entire wafer. The composite wafer has sufficient mechanical strength to support wafer thinning, to withstand subsequent dicing operations, and is clean enough to be taken inside annealing chamber.

Wafer-level thinning consists of etching the handle silicon wafer, using the buried oxide as an etch-stop. We have tried both wet and dry-etching methods. We have used a two-step wafer removal approach – with an initial silicon removal by lapping, wet-etching or by reactive ion etching down to ~ 100 μm thickness. Three different methods were tried for carrying out the final etch, stopping on the buried thermal oxide [7]: (i) hot KOH (50% dilution) wet etch, (ii) inductively coupled plasma RIE with SF_6, and (iii) vapor-phase dry-etching without plasma using XeF_2 gas [8]. While all the etching methods are geared for wafer-level thinning, equipment incompatibilities have forced us to carry out some of the dry-etching on smaller wafer segments. Etching with SF_6 resulted in gross thickness variations across the wafer. The etch-selectivity of SF_6 between Si and SiO_2 is ~ 70:1. Poor etch-selectivity coupled with the non-uniformities of etching resulted

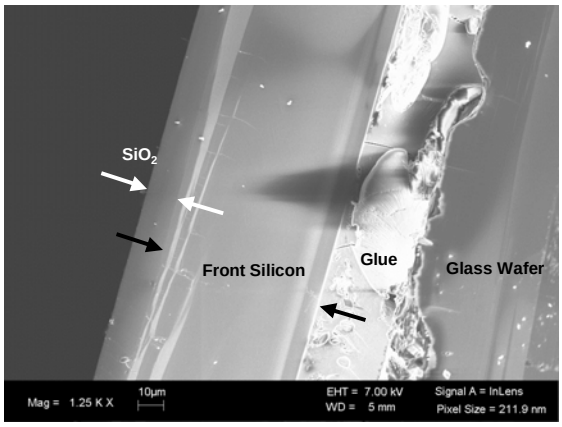

Figure 3: SEM picture of a thinned CMOS imager

in unacceptably high surface roughness, surface thickness variation over a 1 mm x 1mm area being >2000A^{o}. Excellent surface roughness and uniformity control was achieved both by hot-KOH etch and vapor-phase isotropic XeF_2 etch. The latter, having an etch selectivity in excess of 5000:1, produced the most uniform and planar surface, with surface roughness better than 20A (the resolution limit of the AFM probe). Figure 3 is a SEM picture of the cross-section of the imager after the handle-wafer was etched away as part of the backside thinning.

Following thinning, the chip-pads remain buried in the ILD stack under the device silicon and the exposed oxide etch-stop layer. To open the pads, we etch the silicon and SiO_2 from the back (i.e. the illuminated side) of the wafer to expose the belly of the I/O pads [9]. A small aspect ratio for etching (12 μm deep and 300 μm wide) circumvents fabrication difficulties. In addition, metal is deposited and patterned on the back of the silicon wafer both for making backside contacts and for shielding the on-chip support electronics from light. A PECVD nitride layer provides final protective layer, followed by hydrogen anneal for dark current reduction. The nitride layer provides both dark current reduction, and QE enhancement by reducing the interface-state density at the back (illumination side) side Si-SiO_2 interface, as well as by providing a level of anti-reflection coating. Figure 4 shows a picture of the pads at the intersecting corners of four dies, after pad-opening and following the application wafer protection coatings. The wafer is then sawed through the dicing channels, resulting in back-illuminated imager chips that are wire-bonded for electrical and optical tests.

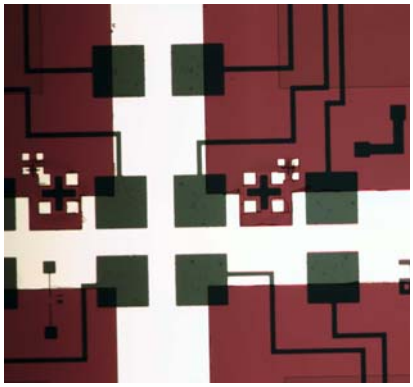

Figure 4: Picture of the wafers after pad-opening step

Figure 5 shows the schematic block-diagram of the digital megapixel CMOS imager. It consists of a pixel array with standard "3T" pixels, in-column gain stages feeding into gain-ranging a 15 bit column-parallel ADC. Careful layout and power routing was adopted to minimize fixed pattern noise (FPN) and gain non-uniformity. The "digital-imager-on-chip", consisting of bias generation circuits, and timing and control digital circuits for autonomous operation, was thinned to demonstrate back-illuminated digital imager technology. The test structures, fabricated at NJIT, consist of individual pixels arranged in a 3x3 blocks, with a readout from the center pixel. Measured data is currently available for the megapixel imager that was thinned with a glued-glass wafer as support, while more extensive backside process variations were carried out on the test structures.

The interface quality of the exposed surface (i.e. the light-gathering surface) is a key element of a back-illuminated imager. Additional boron was added to the device layer right under the buried oxide (BOX) during the starting wafer preparation. The purpose of the added boron layer is to hold the Si-SiO_2 interface between the buried oxide and the device silicon layer in equilibrium (providing low dark current and high blue quantum efficiency), as well as to provide a built-in electric field to suppress cross-talk by reducing lateral diffusion.

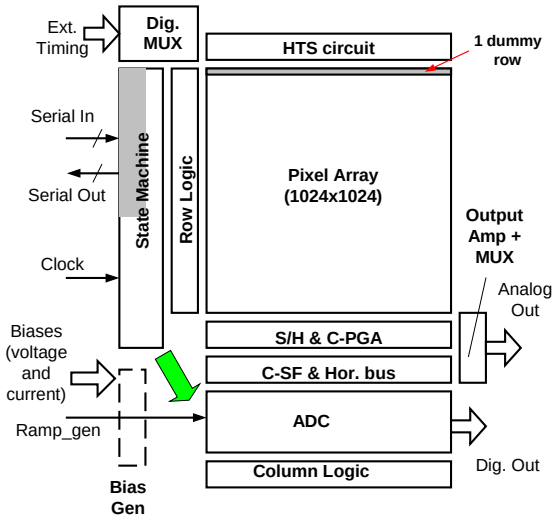

Figure 5: Schematic block diagram of the megapixel digital CMOS imager

Figure 6 shows the measured dark current from the test structure for different variations of the boron content at the back-surface, presence of nitride

Boron content at the top surface	Nitride deposition	H_2 anneal	Dark Current (nA/cm^2)
None	None	None	9.1
Medium	None	None	0.8
Medium	Yes	Yes	0.16
High	Yes	Yes	0.13

Figure 6: Comparison of dark current for different top (exposed) surface conditions (from test structures)

coating on the back-side, and presence or absence of hydrogen anneal. Without the presence of boron at the exposed surface, dark current is extremely high, but is drastically reduced, even with the addition of a moderate amount of boron. By appropriately tailoring the boron concentration at the back-surface, and with the addition of PECVD nitride and H_2 anneal, the dark current can be reduced to acceptable values, typical of "3T" pixels. Thus, good interface quality can be achieved in a back-illuminated imager without requiring complex and non-traditional post-thinning processing such as flash gates, laser anneal, low-pressure oxide deposition, and MBE-based delta-doping [10-14].

Figure 7 shows the measured QE from both the megapixel imager (solid triangles) and test structures. As expected, without the presence of additional boron on the exposed surface, the blue QE is very low, but the green and longer wavelength QE is hardly affected. The blue QE increases almost by a factor of 2 with the increasing boron content. With a multi-layer AR coating, the QE is increased to near 85%. Measured results match quite well with published QE models [15,16]. Further increase in QE is possible with further optimizations in AR coating. Measured PRNU of the back-illuminated megapixel imager is the same as that in the front-illuminated case, and is only 1.4%. Both full well (80,000 e^-) and the read noise (< 7 e^-) with off-chip CDS are independent of operation in the front or back-illuminated mode. The results are strongly suggestive of the maturing of the process technology for implementing high-performance back-illuminated CMOS imagers.

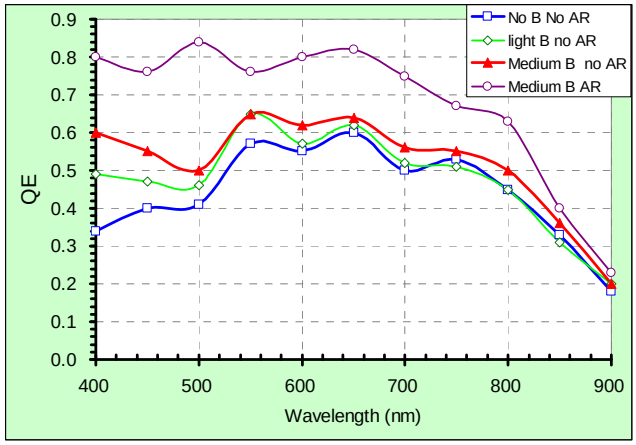

Figure 7: Measured QE for different exposed surface conditions

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References:

1. B. Pain, *2005 IEEE Workshop CCD/AIS*, 2005.
2. S. Iwabuchi et al., *IEEE Intl. Solid-State Circuits Conference*, vol. 49, pp. 302-303, 2006.
3. R. Winzenread, *Proc. SPIE*, vol. 2198, pp. 886-894, 1994.
4. M. Lesser, *Proc. SPIE*, vol. 1447, pp. 177-183, 1991.
5. J.A. Burns et al., *IEEE Trans. Electron Devices*, vol. 53, pp. 2507-2516, 2006.
6. Q.Y.Tong and U. Gosele, in *Semiconductor Wafer Bonding*, The Electrochemical Society Press, pp. 62, 1999.
7. M.J. Madou in *Fundamentals of Microfabrication*, CRC Press, pp. 104-110, 206-211, 2002.
8. F.I. Chang et al., *Proc. SPIE*, vol. 2641, pp. 117-126, 2007.
9. K.W. Gladhill, *Proc. SPIE*, vol. 1656, pp. 585-598, 1992.
10. M. Lesser, *Proc. SPIE*, vol. 2198, pp. 782-791, 1994.
11. J. Janesick et al., *Proc. SPIE*, vol. 982, pp. 543-582, 1986.
12. R.A. Stern et al., *Proc. SPIE*, vol. 1071, pp. 43-57, 1989.
13. J.R. Tower et al., *IEEE Trans. Electron Devices*, vol. 50, pp. 218-224, 2003.
14. S. Nikzad et al., *Proc. of SPIE*, vol. 2198, pp. 907, 1994
15. C.M. Huang et al. *Proc. SPIE*, vol. 1447, pp. 156-164, 1991.
16. M. Blouke et al., *Proc. SPIE*, vol.1447, pp. 142-155, 1991.